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| 10/029,394 | 12/28/2001 | Jum Soo Kim | 054216-5016 | 2075 |

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| EXAMINER | |
|---|---|
| NGUYEN, KHIEM D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2823 | |

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/029,394 | KIM ET AL. | |
| | Examiner | Art Unit | |
| | Khiem D. Nguyen | 2823 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *7-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 14th, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (7-13) are pending in the application.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Fang (U.S. Patent 6,667,511).

In re claim 7, **Fang** discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising:

forming a device isolation film **319** in a given region on a semiconductor substrate **304** to define an active region and a device isolation region (col. 10, lines 6-16 and FIG. 9e);

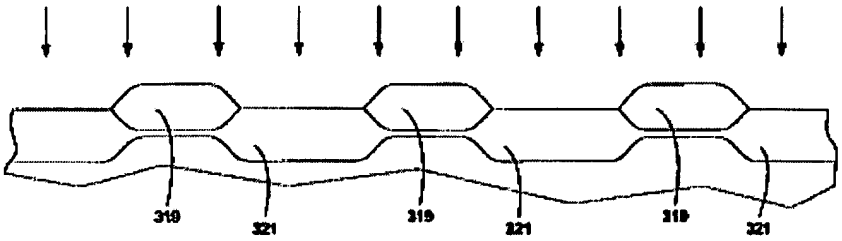


**FIGURE 9e**

defining the active region into a cell region **317** and a peripheral circuit region 314, 315 by a given process;

forming a tunnel oxide film **108** and a first polysilicon film **122** on the entire structure including the device isolation (col. 6, lines 21-44 and FIGS. 5b and 5d) and then

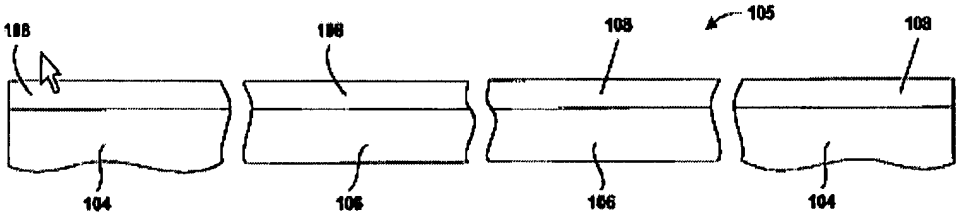


**FIGURE 5b**

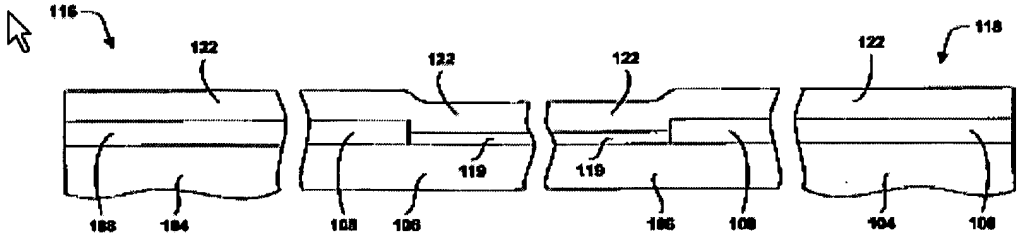


**FIGURE 5d**

patterning the tunnel oxide film **108** and the first polysilicon film **122** so that the tunnel oxide film **108** and the first polysilicon film **122** remain in a given region of the cell region **317**, thus defining a floating gate (col. 6, lines 30-62 and FIG. 5f and col. 7, lines 31-56 and FIG. 9f);

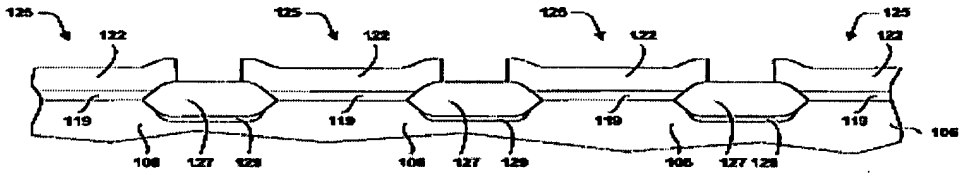

**FIGURE 5f**

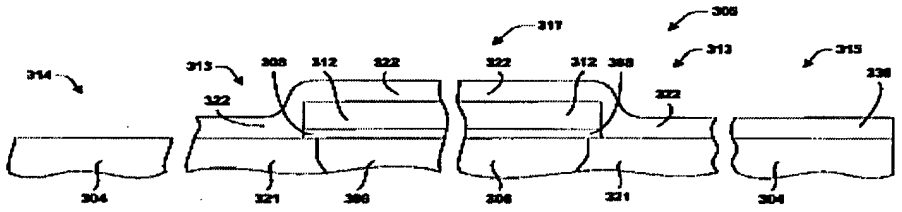

**FIGURE 9f**

sequentially forming an insulating film **322** including an oxide film and a nitride film (ONO) and a second polysilicon film **338** on the entire structure including the cell region **317** and the peripheral circuit region **314, 315**, the insulating film being formed under the second polysilicon film **338** (col. 10, lines 29-65 and FIG. 9g);

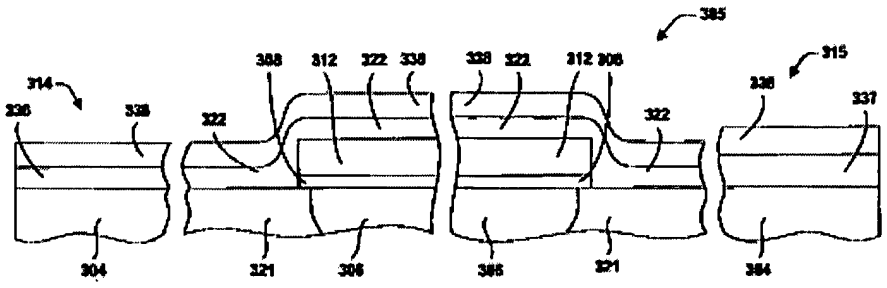

**FIGURE 9g**

patterning the second polysilicon film **338** and the insulating film **322** so that they remain in a given region of the cell region **317** and the peripheral circuit region **314, 315** respectively, thus forming a control gate **338** on the insulating film covering the floating gate **312** in the cell region **317** and a gate on the insulating film covering a surface of the substrate **304** in the peripheral circuit region **314, 315** (col. 10, line 66 to col. 11, line 19 and FIG. 9i); and

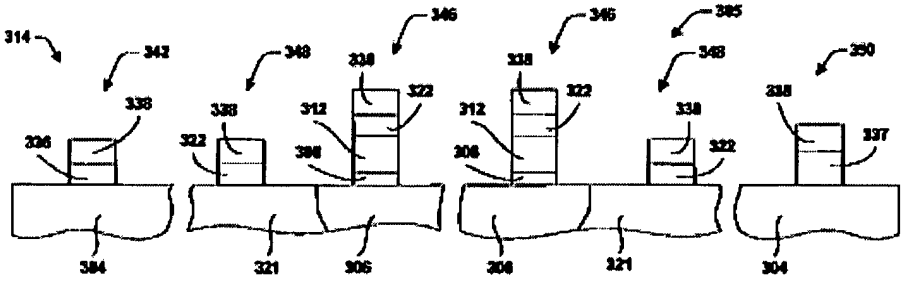

**FIGURE 9i**

performing an impurity ion implantation process for a given region of the semiconductor substrate to form a source region and a drain region , so that a flash memory cell **346** is formed in the cell region, and a code address memory cell **348** is formed in the peripheral circuit region (col. 10, lines 6-16 and FIG. 9i).

In re claims 8 and 10, **Fang** discloses that the insulating film **22** is formed by stacking at least two or more layers of at least one of the oxide and nitride film (col. 10, lines 29-38).

In re claim 9, **Fang** discloses that the insulating film **22** has a thickness of about 130 Angstroms (col. 10, lines 29-38).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U.S. Patent 6,667,511) in view of Sheng et al. (U.S. Patent 5,981,404).

In re claims 11 and 12, **Fang** does not explicitly disclose that the insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film.

**Sheng**, however, discloses a insulating structures used in DRAMs or other memory devices such that the insulating structures is formed by stacking a first oxide film **30**, a first nitride film **32**, a second oxide film **34**, a second nitride film **36** and a third oxide film **34** (col. 7, line 41 to col. 9, line 23 and FIGS. 6 and 9).

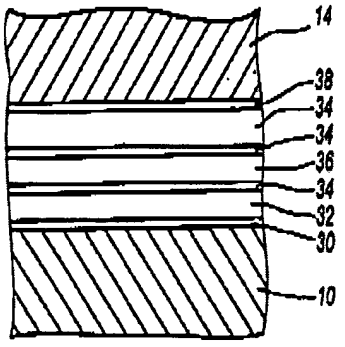


FIG. 6

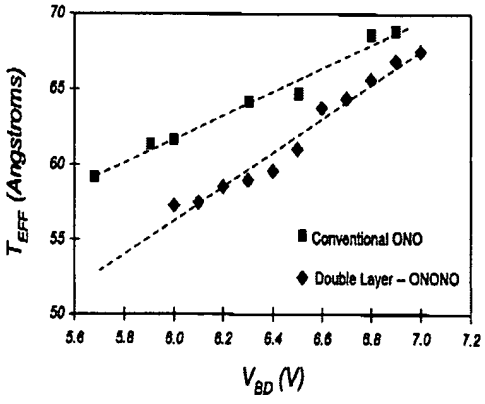


FIG. 9

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Fang and Sheng to enable the process of creating an insulating film formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film of Fang to be performed and furthermore other improvements in the dielectric structure account for the improvements in the breakdown voltage characteristics of the ONONO dielectric structure (col. 9, lines 23-26, Sheng).

In re claim 13, **Fang** discloses a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region, the method comprising the steps of:

forming a device isolation film **319** in a given region on a semiconductor substrate **304** to define an active region and a device isolation region (col. 10, lines 6-16 and FIG. 9e);

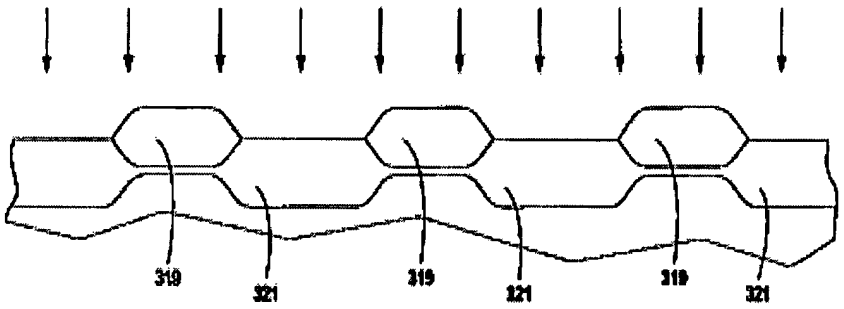


**FIGURE 9e**

defining the active region into a cell region **317** and a peripheral circuit region **314, 315** by a given process;

forming a tunnel oxide film **108** and a first polysilicon film **122** on the entire structure including the device isolation film (col. 6, lines 21-44 and FIGS. 5b and 5d) and then

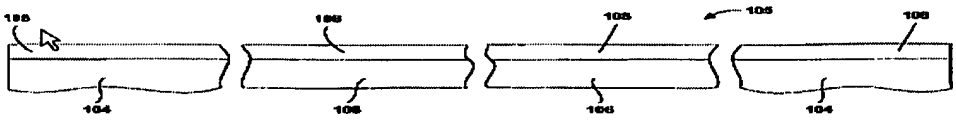

FIGURE 5b

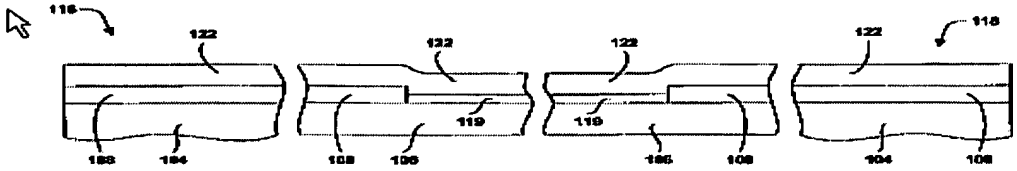

FIGURE 5d

patterning the tunnel oxide film **108** and the first polysilicon film **122** so that the tunnel oxide film **108** and the first polysilicon film **122** only remains in a given region of the cell region **317**, thus defining a floating gate **312** (col. 6, lines 30-62 and FIG. 5f and col. 7, lines 31-56 and FIG. 9f);

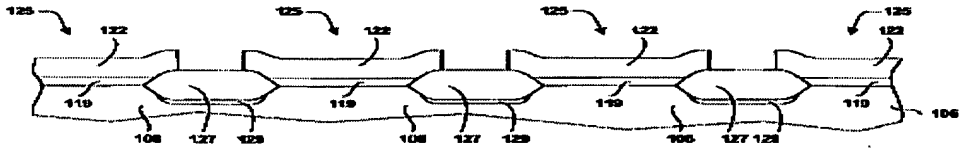

FIGURE 5f

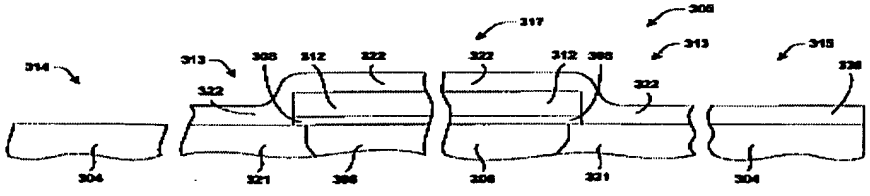

FIGURE 9f

sequentially forming an insulating film **322** including an oxide film and a nitride film (ONO) and a second polysilicon film **338** on the entire structure including the cell region **317** and the peripheral circuit region **314, 315**, the insulating film being formed under the second polysilicon film **338** (col. 10, lines 29-65 and FIG. 9g);

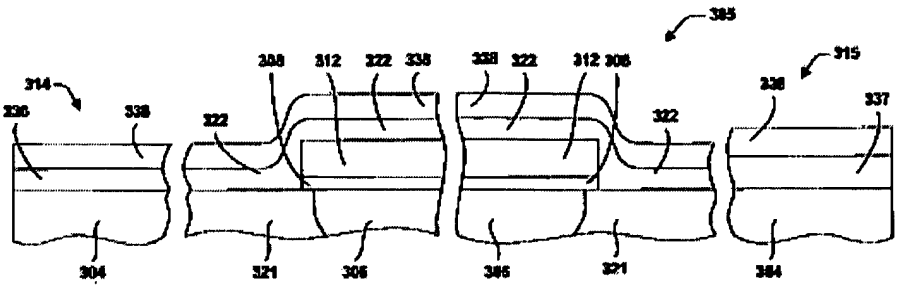

**FIGURE 9g**

patterning the second polysilicon film **338** and the insulating film **322** so that they remain only in a given region of the cell region **317** and the peripheral circuit region **314, 315** respectively, thus forming a control gate **338** of the flash memory cell on the insulating film covering the floating gate **312** in the cell region **317** and a gate on the insulating film covering a surface of the substrate **304** in the peripheral circuit region **314, 315** (col. 10, line 66 to col. 11, line 19 and FIG. 9i); and

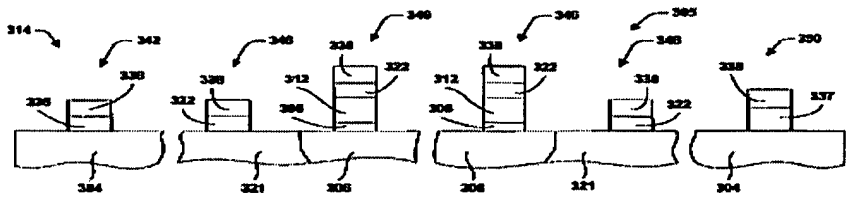

**FIGURE 9i**

performing an impurity ion implantation process for a given region of the semiconductor substrate to form a source region and a drain region, so that a flash

memory cell **346** is formed in the cell region, and a code address memory cell **348** is formed in the peripheral circuit region (col. 10, lines 6-16 and FIG. 9i).

**Fang** does not explicitly discloses that the insulating film is formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film as recited in independent claim 13.

**Sheng**, however, discloses a insulating structures used in DRAMs or other memory devices such that the insulating structures is formed by stacking a first oxide film **30**, a first nitride film **32**, a second oxide film **34**, a second nitride film **36** and a third oxide film **34** (col. 7, line 41 to col. 9, line 23 and FIGS. 6 and 9).

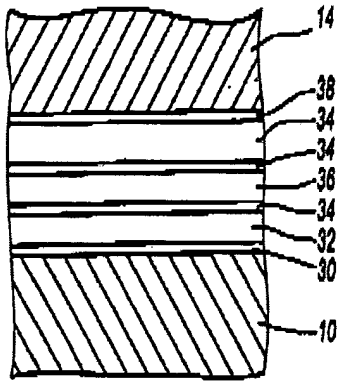


FIG. 6

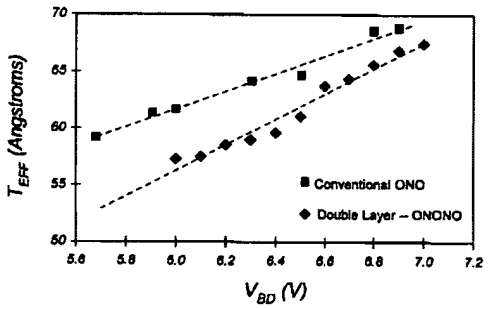


FIG. 9

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Fang and Sheng to enable the process of creating an insulating film formed by stacking a first oxide film, a first nitride film, a second oxide film, a second nitride film and a third oxide film of Fang to be performed and furthermore other improvements in the dielectric structure account for the improvements in the breakdown voltage characteristics of the ONONO dielectric structure can be obtained (col. 9, lines 23-26, Sheng).

***Response to Applicants' Amendment and Arguments***

Applicant contends that the reference Fang (U.S. Patent 6,667,511), herein known as Fang fails to teach, or even suggest, a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region that includes sequentially forming an insulating film including an oxide film and a nitride film and a second polysilicon film on the entire structure including the cell region and the peripheral circuit region and patterning the second polysilicon film and the insulating film so that they remain in a give region of the cell region and the peripheral circuit region respectively.

In response to Applicants' contention that Fang fails to teach, or even suggest, a method of manufacturing a code address memory cell in a peripheral circuit region and a flash memory cell in a cell region that includes sequentially forming an insulating film including an oxide film and a nitride film and a second polysilicon film on the entire structure including the cell region and the peripheral circuit region and patterning the second polysilicon film and the insulating film so that they remain in a give region of the cell region and the peripheral circuit region respectively, Examiner respectfully disagrees.

Applicants are directed to (col. 10, lines 29-65 and FIG. 9g) where Fang discloses sequentially forming an insulating film **322** including an oxide film and a nitride film (ONO) and a second polysilicon film **338** on the entire structure including the cell region **317** and the peripheral circuit region **314, 315**, the insulating film being formed under the second polysilicon film **338**; and (col. 10, line 66 to col. 11, line 19 and FIG. 9i) patterning the second polysilicon film **338** and the insulating film **322** so that they remain

in a given region of the cell region **317** and the peripheral circuit region **314, 315** respectively, thus forming a control gate **338** on the insulating film covering the floating gate **312** in the cell region **317** and a gate on the insulating film covering a surface of the substrate **304** in the peripheral circuit region **314, 315**.

For this reason, Examiner holds the rejection proper.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
January 21, 2006

W. DAVID COLEMAN
PRIMARY EXAMINER